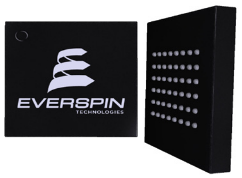
EVERSPIN®
TECHNOLOGIES
The MRAM Company™

MR2A08A

512K x 8 MRAM Memory

FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20 years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to eliminate battery assembly, improving reliability
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Automotive Temperatures
- **RoHS-Compliant** SRAM TSOP2 Package
- **RoHS-Compliant** SRAM BGA Package
- AEC-Q100 Grade 1 Qualified



INTRODUCTION

The **MR2A08A** is a 4,194,304-bit magnetoresistive random access memory (MRAM) device organized as 524,288 words of 8 bits. The MR2A08A offers SRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20 years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification.

The MR2A08A is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The **MR2A08A** is available in a small footprint 400-mil, 44-lead plastic small-outline TSOP type 2 package or an 8 mm x 8 mm, 48-pin ball grid array (BGA) package with 0.75 mm ball centers. These packages are compatible with similar low-power SRAM products and other non-volatile RAM products.

The **MR2A08A** provides highly reliable data storage over a wide range of temperatures. The product is offered with commercial temperature range (0 to +70 °C), industrial temperature range (-40 to +85 °C), and AEC-Q100 Grade 1 temperature range (-40 to +125 °C) options.

CONTENTS

1. DEVICE PIN ASSIGNMENT

Figure 1.1 Block Diagram

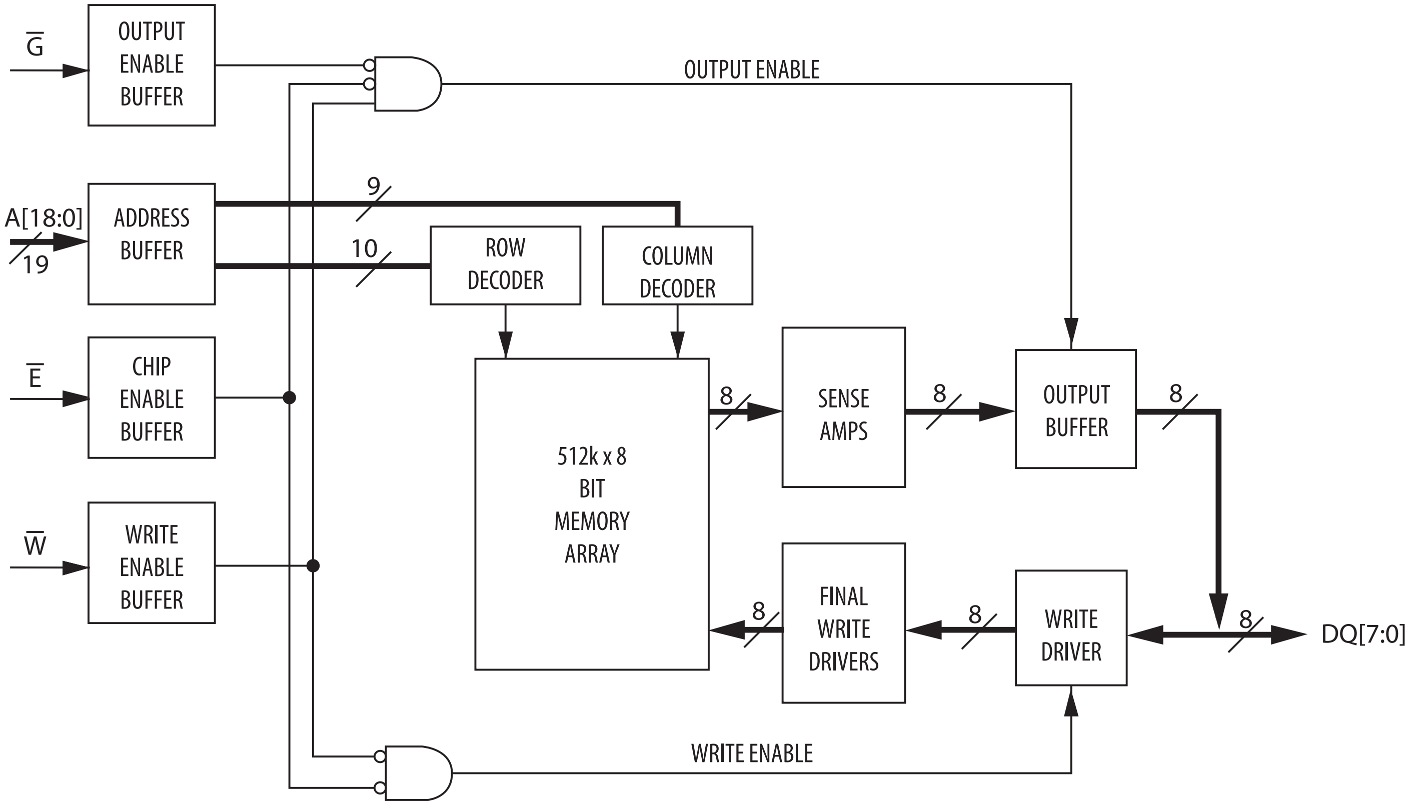
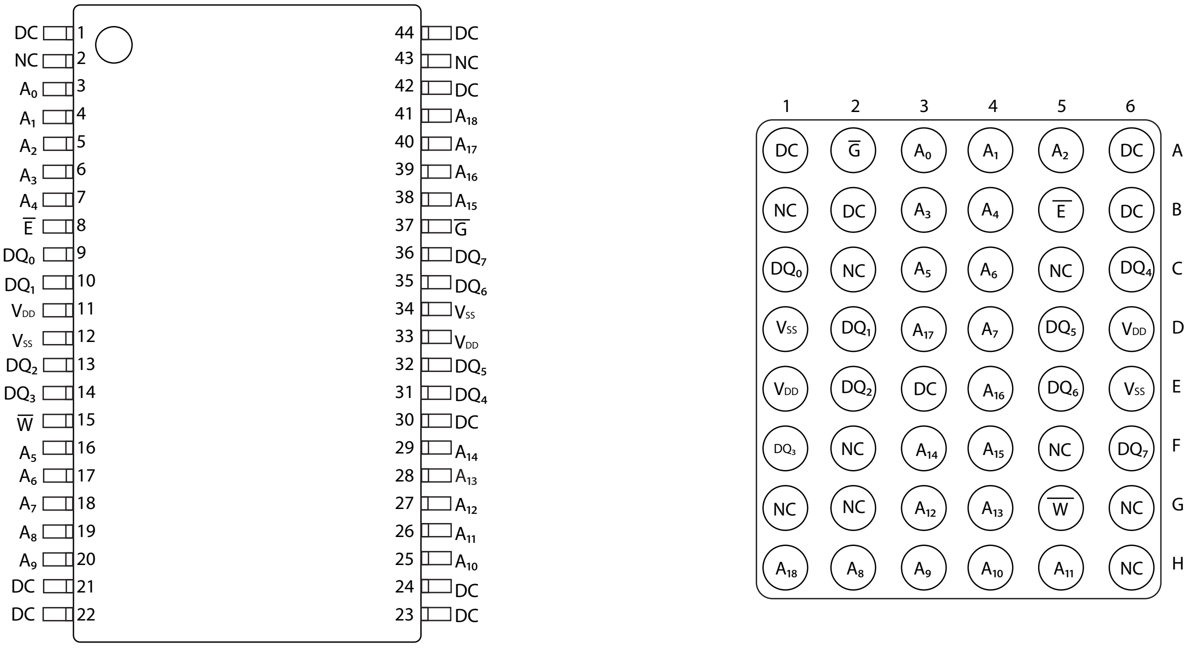


Table 1.1 Pin Functions

Signal Name	Function
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ	Data I/O
V_{DD}	Power Supply
V_{SS}	Ground
DC	Do Not Connect
NC	No Connection - Pin 2, 43 (TSOPII); Ball H6, G2 (BGA) Reserved For Future Expansion

Figure 1.2 Pin Diagrams for Available Packages (Top View)



44 Pin TSOP2 **48 Pin FBGA**

Table 1.2 Operating Modes

$\overline{\text{E}}$[1]	$\overline{\text{G}}$[1]	$\overline{\text{W}}$[1]	Mode	V_{DD} Current	DQ[7:0][2]
H	X	X	Not selected	I_{SB1}, I_{SB2}	Hi-Z
L	H	H	Output disabled	I_{DDR}	Hi-Z
L	L	H	Byte Read	I_{DDR}	D_{Out}
L	X	L	Byte Write	I_{DDW}	D_{in}

[1] H = high, L = low, X = don't care

[2] Hi-Z = high impedance

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2.1 Absolute Maximum Ratings[1]

Symbol	Parameter	Temp Range	Package	Value	Unit
V_{DD}	Supply voltage [2]	-	-	-0.5 to 4.0	V
V_{IN}	Voltage on any pin [2]	-	-	-0.5 to V_{DD} + 0.5	V
I_{OUT}	Output current per pin	-	-	±20	mA
P_D	Package power dissipation [3]	-	Note 3	0.600	W
T_{BIAS}	Temperature under bias	Commercial	-	-10 to 85	°C
		Industrial	-	-45 to 95	
		AEC-Q100 Grade 1	-	-45 to 130	
T_{stg}	Storage Temperature	-	-	-55 to 150	°C
T_{Lead}	Lead temperature during solder (3 minute max)	-	-	260	°C
H_{max_write}	Maximum magnetic field during write	Commercial	TSOP2, BGA	2,000	A/m
		Industrial	BGA	2,000	
			TSOP2	10,000	
		AEC-Q100 Grade 1	TSOP2	2,000	
H_{max_read}	Maximum magnetic field during read or standby	Commercial	TSOP2, BGA	8,000	A/m
		Industrial	BGA	8,000	
			TSOP2	10,000	
		AEC-Q100 Grade 1	TSOP2	8,000	

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability depends on package characteristics and use environment.

Table 2.2 Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage [1]	V_{DD}	3.0	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0 [1]	V
Input high voltage	V_{IH}	2.2	-	V_{DD} + 0.3 [2]	V
Input low voltage	V_{IL}	-0.5 [3]	-	0.8	V
Temperature under bias	T_A				°C
MR2A08A (Commercial)		0		70	
MR2A08AC (Industrial)		-40		85	
MR2A08AM (AEC-Q100 Grade 1)[4]		-40		125	

[1] There is a 2 ms startup time once V_{DD} exceeds $V_{DD,}$(min). See **Power Up and Power Down Sequencing** below.

[2] $V_{IH}(\max) = V_{DD} + 0.3\ V_{DC}$; $V_{IH}(\max) = V_{DD} + 2.0\ V_{AC}$ (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

[3] $V_{IL}(\min) = -0.5\ V_{DC}$; $V_{IL}(\min) = -2.0\ V_{AC}$ (pulse width ≤ 10 ns) for I ≤ 20.0 mA.

[4] AEC-Q100 Grade 1 temperature profile assumes 10% duty cycle at maximum temperature (2-years out of 20-year life)

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time.

During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

Figure 2.1 Power Up and Power Down Diagram

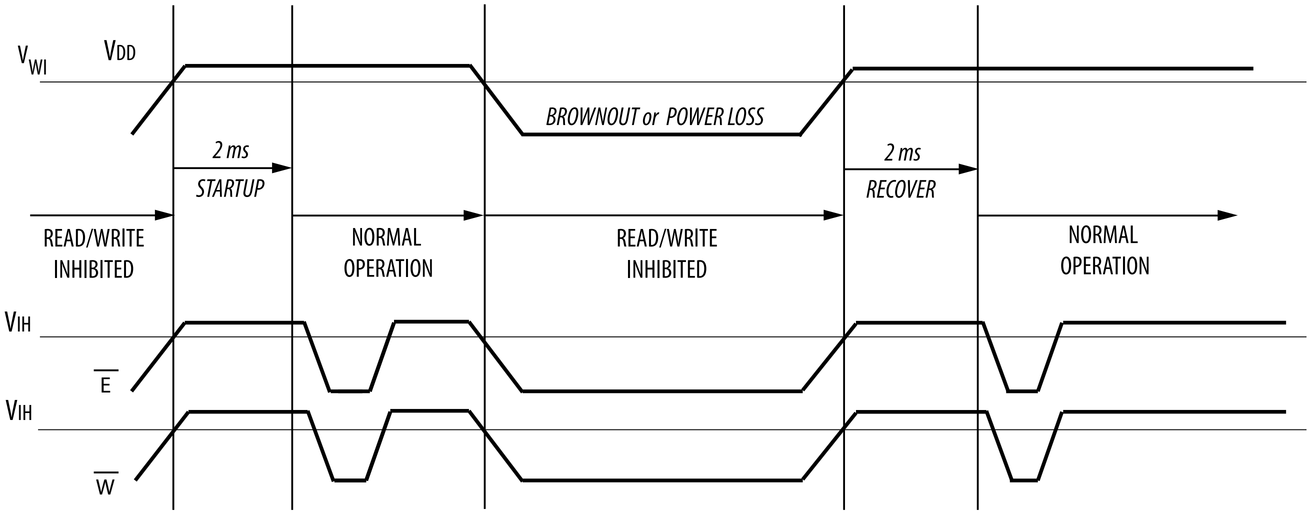


Table 2.3 DC Characteristics

Parameter	Symbol	Min	Max	Unit
Input leakage current	$I_{lkg(I)}$	-	±1	µA
Output leakage current	$I_{lkg(O)}$	-	±1	µA
Output low voltage (I_{OL} = +4 mA) (I_{OL} = +100 µA)	V_{OL}	-	0.4 V_{SS} + 0.2	V
Output high voltage (I_{OL} = -4 mA) (I_{OL} = -100 µA)	V_{OH}	2.4 V_{DD} - 0.2	-	V

Table 2.4 Power Supply Characteristics

Parameter	Symbol	Typical	Max	Unit
AC active supply current - read modes[1] (I_{OUT}= 0 mA, V_{DD}= max)	I_{DDR}	30	66	mA
AC active supply current - write modes[1] (V_{DD}= max) Commercial Grade Industrial Grade AEC-Q100 Grade	I_{DDW}	90 90 90	135 135 135	mA
AC standby current (V_{DD}= max, $\overline{E} = V_{IH}$) *no other restrictions on other inputs*	I_{SB1}	13	20	mA
CMOS standby current ($\overline{E} \geq V_{DD}$ - 0.2 V and $V_{In} \leq V_{SS}$ + 0.2 V or $\geq V_{DD}$ - 0.2 V) (V_{DD} = max, f = 0 MHz)	I_{SB2}	8	10	mA

[1] All active current measurements are measured with one address transition per cycle and at minimum cycle time.

3. TIMING SPECIFICATIONS

Table 3.1 Capacitance[1]

Parameter	Symbol	Typical	Max	Unit
Address input capacitance	C_{In}	-	6	pF
Control input capacitance	C_{In}	-	6	pF
Input/Output capacitance	$C_{I/O}$	-	8	pF

[1] f = 1.0 MHz, dV = 3.0 V, T_A = 25 °C, periodically sampled rather than 100% tested.

Table 3.2 AC Measurement Conditions

Parameter	Value	Unit
Logic input timing measurement reference level	1.5	V
Logic output timing measurement reference level	1.5	V
Logic input pulse levels	0 or 3.0	V
Input rise/fall time	2	ns
Output load for low and high impedance parameters	See Figure 3.1	
Output load for all other timing parameters	See Figure 3.2	

Figure 3.1 Output Load Test Low and High

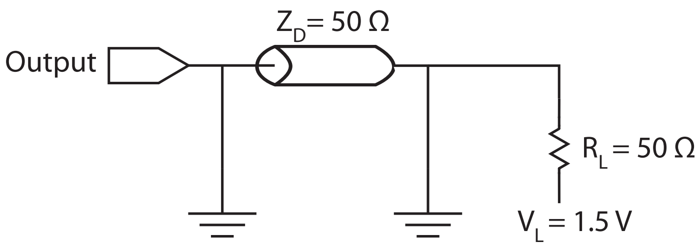
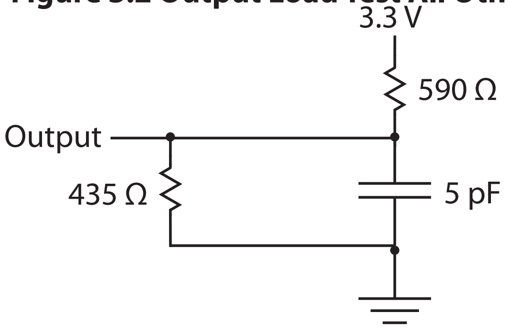


Figure 3.2 Output Load Test All Others



Read Mode

Table 3.3 Read Cycle Timing[1]

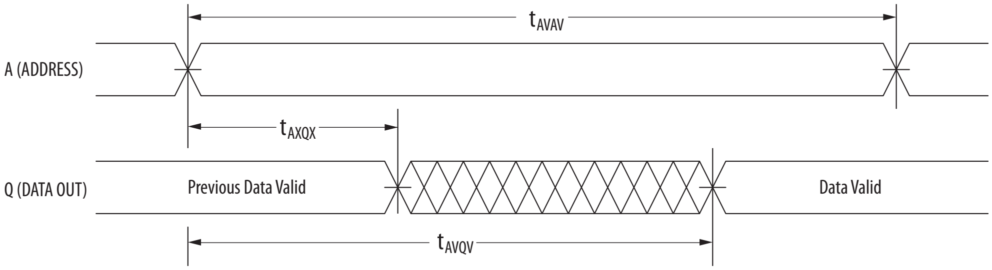
Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{AVAV}	35	-	ns
Address access time	t_{AVQV}	-	35	ns
Enable access time[2]	t_{ELQV}	-	35	ns
Output enable access time	t_{GLQV}	-	15	ns
Output hold from address change	t_{AXQX}	3	-	ns
Enable low to output active[3]	t_{ELQX}	3	-	ns
Output enable low to output active[3]	t_{GLQX}	0	-	ns
Enable high to output Hi-Z[3]	t_{EHQZ}	0	15	ns
Output enable high to output Hi-Z[3]	t_{GHQZ}	0	10	ns

[1] $\overline{W}$ is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.

[2] Addresses valid before or at the same time $\overline{E}$ goes low.

[3] This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage.

Figure 3.3A Read Cycle 1



Note: Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

Figure 3.3B Read Cycle 2

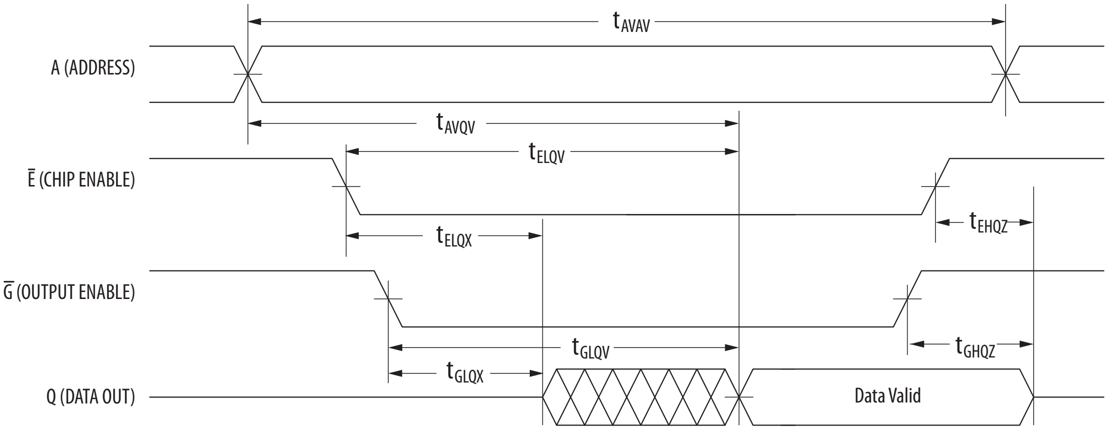


Table 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)[1]

Parameter	Symbol	Min	Max	Unit
Write cycle time [2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVWL}	0	-	ns
Address valid to end of write ($\overline{G}$ high)	t_{AVWH}	18	-	ns
Address valid to end of write ($\overline{G}$ low)	t_{AVWH}	20	-	ns
Write pulse width ($\overline{G}$ high)	t_{WLWH} t_{WLEH}	15	-	ns
Write pulse width ($\overline{G}$ low)	t_{WLWH} t_{WLEH}	15	-	ns
Data valid to end of write	t_{DVWH}	10	-	ns
Data hold time	t_{WHDX}	0	-	ns
Write low to data Hi-Z [3]	t_{WLQZ}	0	12	ns
Write high to output active [3]	t_{WHQX}	3	-	ns
Write recovery time	t_{WHAX}	12	-	ns

[1] All write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If $\overline{G}$ goes low at the same time or after $\overline{W}$ goes low, the output will remain in a high impedance state. After $\overline{W}$ or $\overline{E}$ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between $\overline{E}$ being asserted low in one cycle to $\overline{E}$ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

[3] This parameter is sampled and not 100% tested. Transition is measured ±200 mV from the steady-state voltage. At any given voltage or temperature, t_{WLQZ}(max) < t_{WHQX}(min)

Figure 3.4 Write Cycle Timing 1 ($\overline{W}$ Controlled)

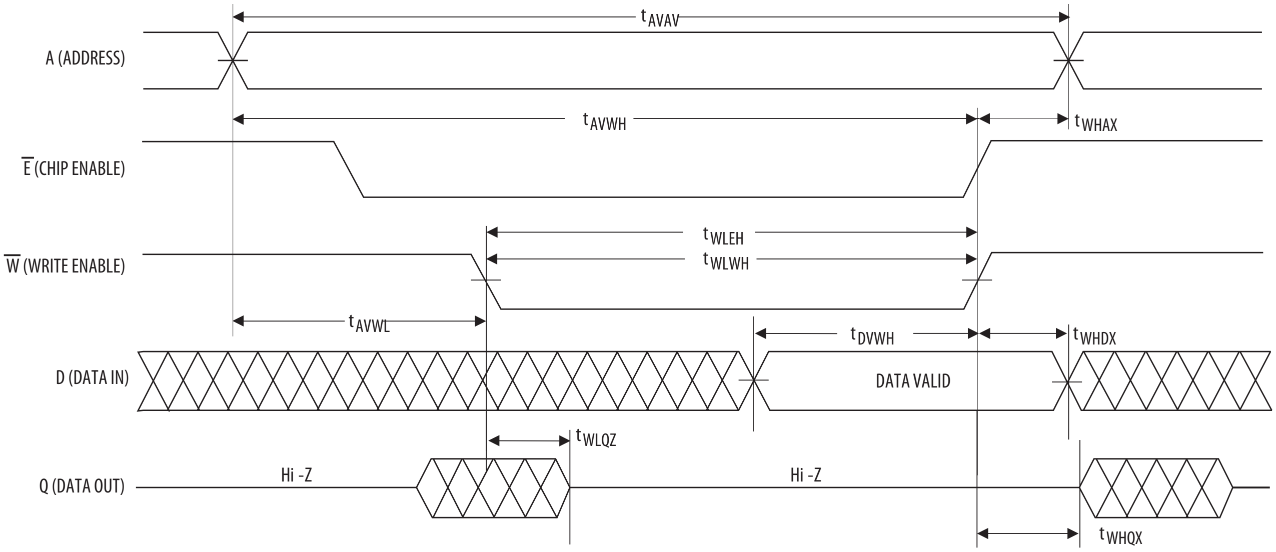


Table 3.5 Write Cycle Timing 2 (E̅ Controlled) [1]

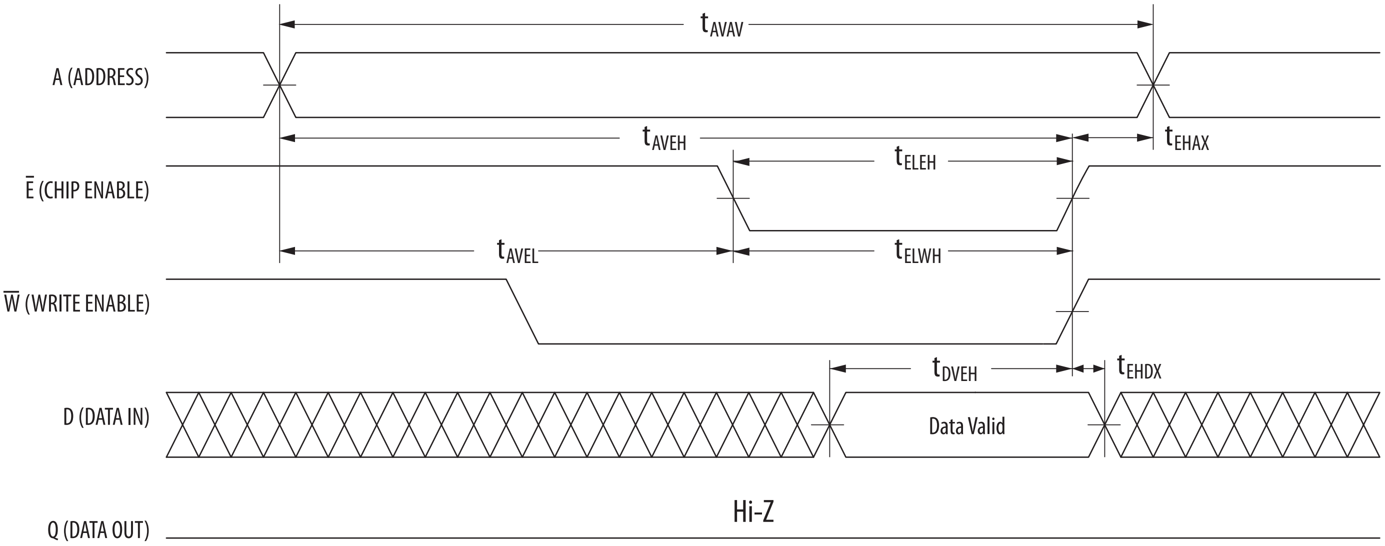
Parameter	Symbol	Min	Max	Unit
Write cycle time [2]	t_{AVAV}	35	-	ns
Address set-up time	t_{AVEL}	0	-	ns
Address valid to end of write (G̅ high)	t_{AVEH}	18	-	ns
Address valid to end of write (G̅ low)	t_{AVEH}	20	-	ns
Enable to end of write (G̅ high)	t_{ELEH} t_{ELWH}	15	-	ns
Enable to end of write (G̅ low) [3]	t_{ELEH} t_{ELWH}	15	-	ns
Data valid to end of write	t_{DVEH}	10	-	ns
Data hold time	t_{EHDX}	0	-	ns
Write recovery time	t_{EHAX}	12	-	ns

[1] All write occurs during the overlap of E̅ low and W̅ low. Power supplies must be properly grounded and decoupled and bus contention conditions must be minimized or eliminated during read and write cycles. If G̅ goes low at the same time or after W̅ goes low, the output will remain in a high impedance state. After W̅ or E̅ has been brought high, the signal must remain in steady-state high for a minimum of 2 ns. The minimum time between E̅ being asserted low in one cycle to E̅ being asserted low in a subsequent cycle is the same as the minimum cycle time allowed for the device.

[2] All write cycle timings are referenced from the last valid address to the first transition address.

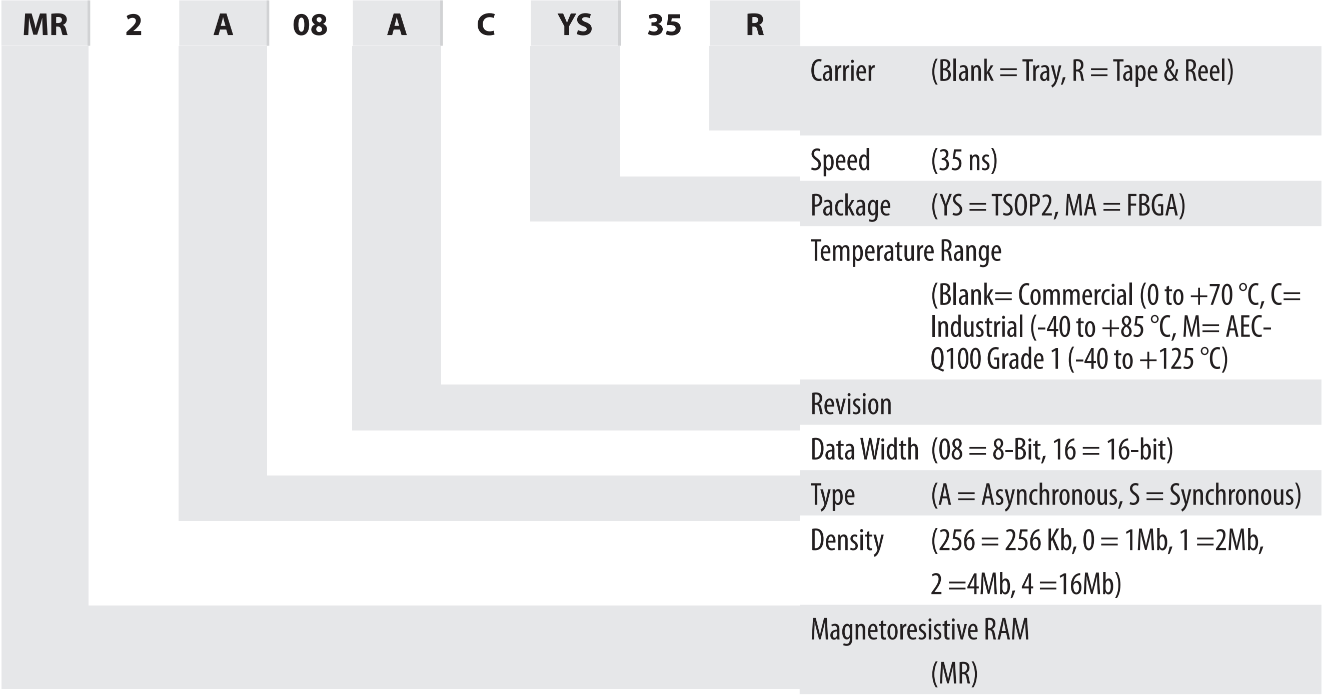
[3] If E goes low at the same time or after W goes low, the output will remain in a high-impedance state. If E goes high at the same time or before W goes high, the output will remain in a high-impedance state.

Figure 3.5 Write Cycle Timing 2 (E̅ Controlled)



4. ORDERING INFORMATION

Figure 4.1 Part Numbering System



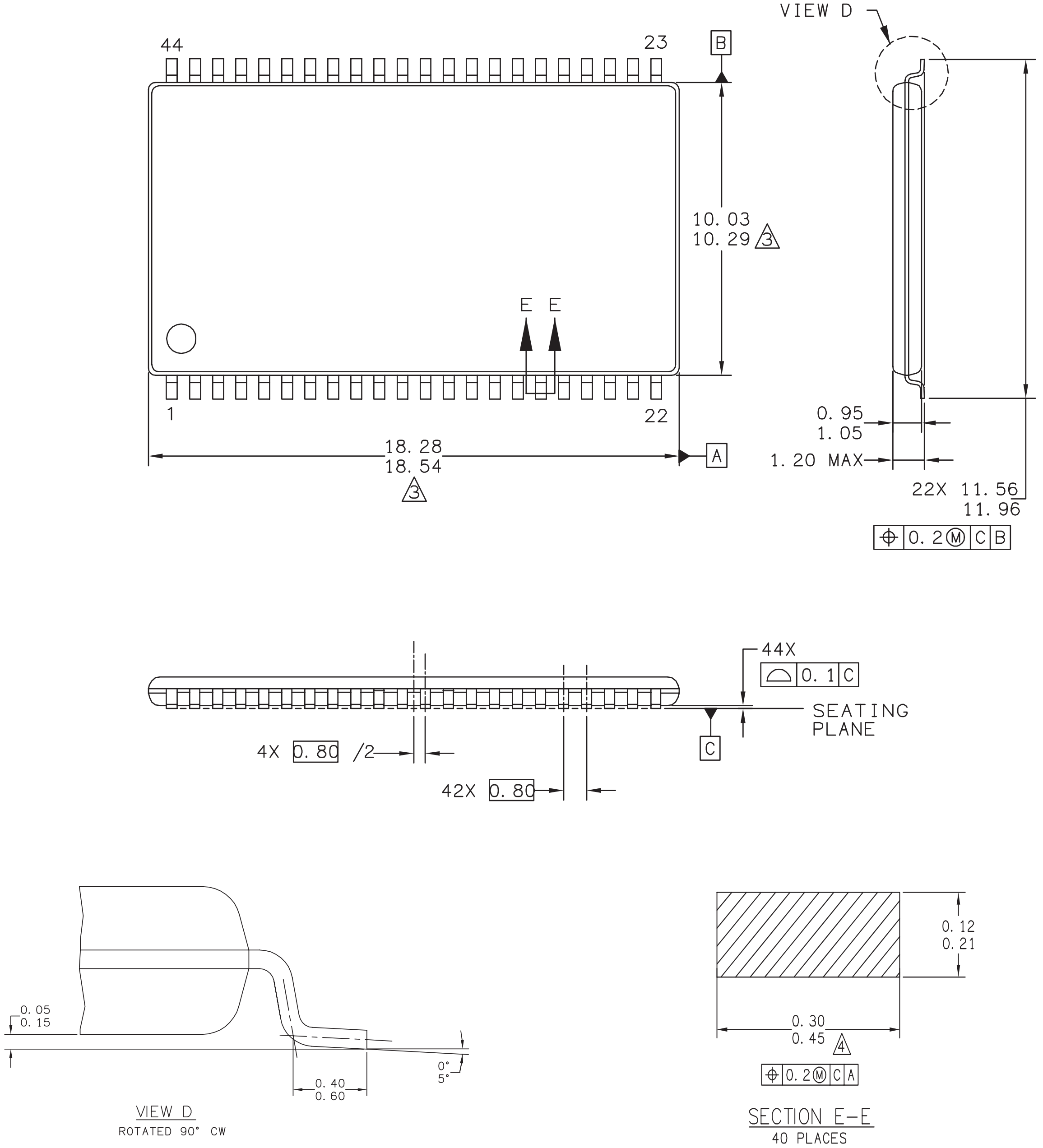
Carrier	(Blank = Tray, R = Tape & Reel)
Speed	(35 ns)
Package	(YS = TSOP2, MA = FBGA)
Temperature Range	(Blank= Commercial (0 to +70 °C, C= Industrial (-40 to +85 °C, M= AEC-Q100 Grade 1 (-40 to +125 °C)
Revision	
Data Width	(08 = 8-Bit, 16 = 16-bit)
Type	(A = Asynchronous, S = Synchronous)
Density	(256 = 256 Kb, 0 = 1Mb, 1 =2Mb, 2 =4Mb, 4 =16Mb)
Magnetoresistive RAM	(MR)

Table 4.1 Available Parts

Part Number	Description	Package	Ship Pack	Temp Range
MR2A08AYS35	3.3 V 512Kx8 MRAM Commercial	44-TSOP2	Tray	0 to +70 °C
MR2A08ACYS35	3.3 V 512Kx8 MRAM Industrial	44-TSOP2	Tray	-40 to +85 °C
MR2A08AMYS35	3.3 V 512Kx8 MRAM AEC-Q100 Grade 1	44-TSOP2	Tray	-40 to +125 °C
MR2A08AYS35R	3.3 V 512Kx8 MRAM Commercial	44-TSOP2	Tape & Reel	0 to +70 °C
MR2A08ACYS35R	3.3 V 512Kx8 MRAM Industrial	44-TSOP2	Tape & Reel	-40 to +85 °C
MR2A08AMYS35R	3.3 V 512Kx8 MRAM AEC-Q100 Grade 1	44-TSOP2	Tape & Reel	-40 to +125 °C
MR2A08AMA35	3.3 V 512Kx8 MRAM Commercial	48-BGA	Tray	0 to +70 °C
MR2A08ACMA35	3.3 V 512Kx8 MRAM Industrial	48-BGA	Tray	-40 to +85 °C
MR2A08AMA35R	3.3 V 512Kx8 MRAM T&R Commercial	48-BGA	Tape & Reel	0 to +70 °C
MR2A08ACMA35R	3.3 V 512Kx8 MRAM T&R Industrial	48-BGA	Tape & Reel	-40 to +85 °C

5. MECHANICAL DRAWING

Figure 5.1 TSOP2

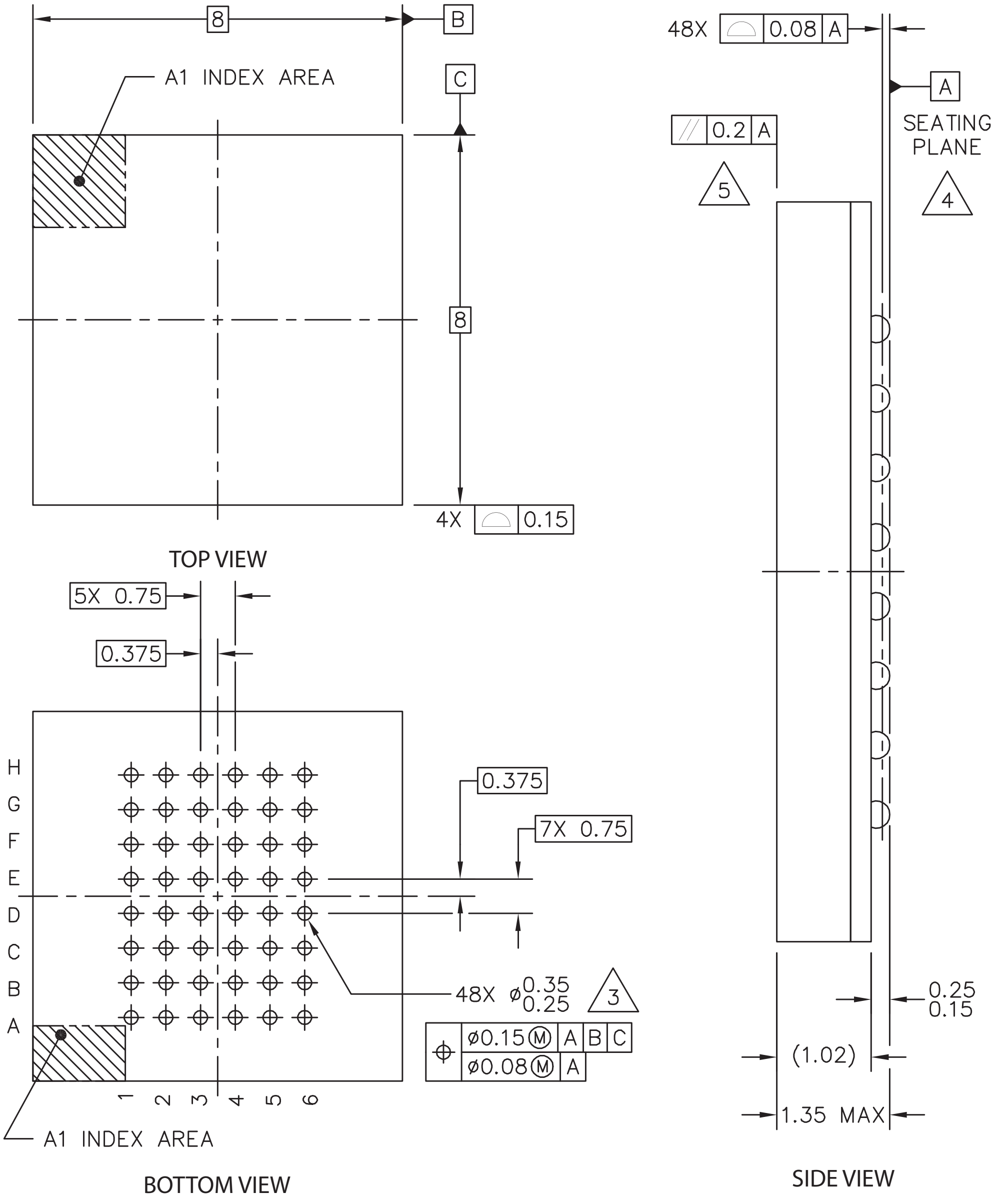


Print Version Not To Scale

1. Dimensions and tolerances per ASME Y14.5M - 1994.
2. Dimensions in Millimeters.
3. Dimensions do not include mold protrusion.
4. Dimension does not include DAM bar protrusions.

DAM Bar protrusion shall not cause the lead width to exceed 0.58.

Figure 5.2 FBGA



Print Version Not To Scale

1. Dimensions in Millimeters.
2. Dimensions and tolerances per ASME Y14.5M - 1994.
3. Maximum solder ball diameter measured parallel to DATUM A
4. DATUM A, the seating plane is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

6. REVISION HISTORY

Revision	Date	Description of Change
1	Oct 29, 2007	Designate pin 23, 24, 42 of TSOPII as DC "Don't Connect" pins since these pins should remain floating at all times. Functional operation of E2 pin defined.
2	Sep 12, 2008	Reformat Datasheet for Everspin, Delete E2 pin Function, Add BGA Package Information Add Tape & Reel Part Numbers, Add Power Sequencing Info, Correct IOH Spec For VOH to -100 uA, Correct ac Test Conditions
3	Apr 10, 2009	Add typical and worst case current specifications
4	July 6, 2009	Changed datasheet from Preliminary to Production except where noted. Updated format.
5	Dec 16, 2011	Added AEC-Q100 Grade 1 temp performance specifications to Table 2.1, Table 2.2, addition of AEC-Q100 Grade 1 and revision of I_{DDW} Typical values in Table 2.4. AEC-Q100 Grade 1 ordering options added to Figure 4.1 and Table 4.1. Changed TSOP-II to TSOP2 everywhere. New logo design. Cosmetic revision to Table 2.1.
6	August 2, 2012	Improved magnetic immunity for Industrial and Extended Grades. Revised Power Up/Power Down Diagram.
6.1	May 19, 2015	Revised contact information.
6.2	June 11, 2015	Corrected Japan Sales Office telephone number.

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